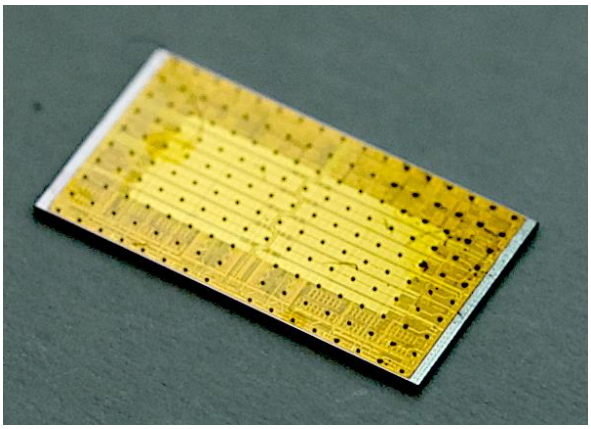
KU1500 Analog Canceller IC
Product Brief



Overview

KU1500 is a chip-scale implementation of frequency agnostic taps for analog self-interference cancellation or analog FIR filtering. Figure 1 shows a system view of a general self-interference cancellation system using the KU1500 IC along with optional frequency specifics taps and digital taps (available separately from Kumu).

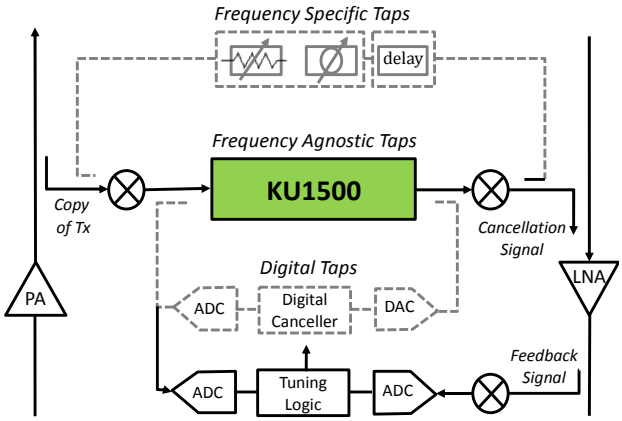


Figure 1: Self-Interference Cancellation System

Frequency specific taps can be used to increase overall dynamic range and where transmit power is higher than what the KU1500 can support. Digital cancellation taps can be used where Analog Cancellation alone does not provide sufficient cancellation depth or where longer delay reflections impact the receiver and need to be cancelled to meet radio performance specifications .

The KU1500 has 4 analog FIR filter chains organized as 12 programmable taps per chain with a maximum of 350ns aggregate delay through each chain. Two chains can be cascaded for a maximum of 24 taps for a total delay of up to 700ns. Alternatively, the chains can be configured to support 2x2 MIMO operation.

The IC supports a range of signal processing applications where analog signal manipulation is required to avoid the delay and resolution problems that digital conversion introduces. For example, the chip can be used to implement full-duplex systems or to improve co-existence between co-located radios.

Features

- Baseband analog canceller integrated circuit providing programmable, frequency agnostic cancellation
- > 45dB Analog Cancellation
- Upto 75dB linearity (IM3)
- Upto -10dBm input & output power
- Upto 700ns delay spread
- Upto 80MHz cancellation bandwidth
- 2Tx 2Rx MIMO or SISO modes
- Simple, high-speed SPI interface with API for real-time tuning adjustments, gain control and configuration
- Integrated DC Offset correction
- Small Size: 4.75mm x 8.5mm x 0.2mm 167-pin CSP package

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Modes of Operation

Parameter	Mode-1	Mode-2	Mode-3	Units
Bandwidth	20	40	80	MHz
Delay per Tap (Taps 1-3)[1],[2]	10	5	2.5	ns
Delay per Tap (Taps 4-11)[2]	40	20	10	ns
Delay spread per Chain (no delay chaining)	350	175	87.5	ns
Delay spread per Chain (with delay chaining)	700	350	175	ns
Output Noise Density @ 1KHz[3]	45			nV/√Hz

[1] Tap 0 has no delay
[2] Nominal delay at 5MHz
[3] FIR Chain only, excludes contribution/benefit from input gain stage

General Parameters

Parameter	Min	Typ	Max	Units
Input Power to IC			-10	dBm
Output Power from IC			-10	dBm
Operating Temperature	-20		70	C

Pin Description

Pin Name	Description
IN_0[3:0]	IF Differential I&Q Inputs Ch1
IN_1[3:0]	IF Differential I&Q Inputs Ch2
OUT_0[3:0]	IF Differential I&Q Output Ch1
OUT_1[3:0]	IF Differential I&Q Output Ch2
SPI_CS	SPI Chip Select
SPI_MISO	SPI Master-in Slave-Out Data
SPI_MOSI	SPI Master-out Slave-in Data
APLS	Apply state
SPI_CLK	SPI Clock
RST_B	Chip Reset
V15	1.5V Power Supply
V25	2.5V Power Supply
GND	Ground

Chip Functional Block Diagram

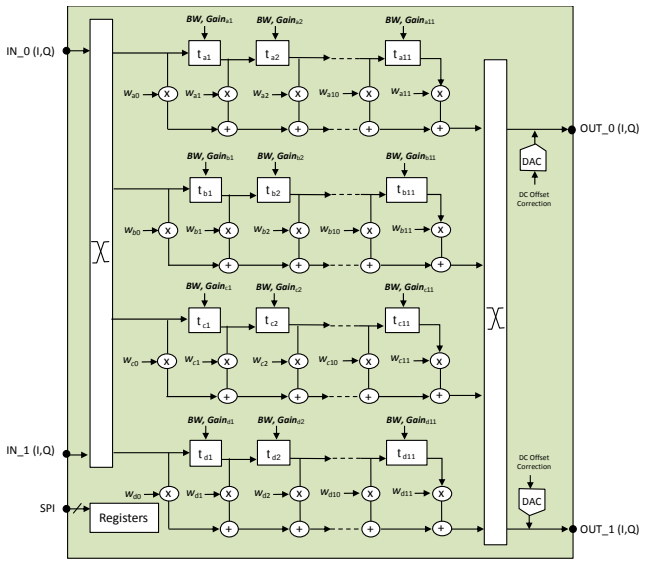
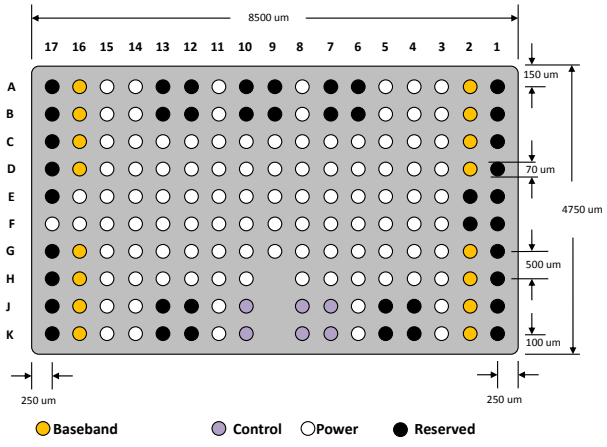


Figure 2: KU1500 Functional Block Diagram

Package



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